Amendments to the Specification:

Please replace the paragraph beginning at page 10, line 16 with the following amended paragraph:

A circuit configuration of the present invention will be described with reference to FIG. 1. FIG. 1 shows pixels and a driving circuit of the present embodiment mode. In FIG. 1, pixels are arranged in a matrix (m columns x n rows) in a pixel portion. An address of a pixel disposed in an i-th column and in a j-th row is represented as (i,j) (i is an integer of 1 to **[[n]]** m, and j is an integer of 1 to **[[m]]** n).

Please replace the paragraph beginning at page 18, line 15 with the following amended paragraph:

FIG. 5 shows Embodiment Mode 2 of the present invention. In FIG. 5, a plurality of address decoders, i.e., a first Y address decoder and a second Y address decoder are provided. In FIG. 5, the address of a pixel arranged in an i-th column and a j-th row is represented as (i, j) (i is an integer of 1 to **[[n]]** m, and j is an integer of 1 to **[[m]]** n).